REMARKS

Claims 1-14 and 16-30 were previously pending in this application. Claims 1, 6-8, 10-11, 13-14, 16-17, 20-21, and 28 are amended herein. Claim 27 is cancelled herein. As a result claims 1-14, 16-26, and 28-30 are pending for examination with claims 1, 8, 16, 22, and 28 being independent claims. No new matter has been added.

Rejections Under 35 U.S.C. §102

The Examiner rejected claims 1-14 and 16-30 under 35 U.S.C. §102(b) as being anticipated by Lee (EP 1 017 183 A2). Applicants respectfully disagrees and traverses as follows.

The Examiner cites Lee for the proposition that it "discloses a method for the despreading of spread spectrum signals in a digital signal processor...performed in response to the generation to the single instruction." (Office Action at 2). While Lee does disclose a method for despreading of spread spectrum signals, and does disclose performing certain operations in response to a single instruction, the execution of the single instruction of Lee does not perform the operations required by Applicants' claims to be executed in a single instruction, nor does Lee disclose performing those operations in a single clock cycle, as required by Applicants' claims. Indeed, the system disclosed in Lee performs its operations one symbol at a time and is therefore incapable of performing the operations required by Applicants' claims in response to a single instruction and in a single clock cycle.

Applicants' claims require performing multiple functions in response to a single instruction within a single clock cycle. For example, claim 1 as amended requires a method comprising:

> in response to a single instruction that specifies a plurality of signal values, each signal value comprising a real component and an imaginary component, and a plurality of code segments of a despreading code:
>
> complex multiplication of each signal value by a respective one of the code segments to provide a plurality of intermediate results;
>
> complex addition of the intermediate results to provide a despread result; and

storing the despread result, wherein the complex multiplication, the complex addition and the storing of the despread result are executed in a single clock cycle of the digital signal processor.

Lee does not disclose a single instruction specifying performing the above operations on a plurality of signal values, each comprising a real component and an imaginary component and a plurality of code segments, nor does Lee disclose performing complex multiplication, addition and storing operations on the plurality of signal values and the plurality of code segments all within a single clock cycle, as claimed. Furthermore, Lee does not disclose operating on signal values which comprise multiple real bits and multiple imaginary bits.

The "single instruction" disclosed by Lee, and cited by the Examiner, is an instruction that operates on only one signal value (comprising only a single real bit and single imaginary bit) at a time. Because of this mode of operation, multiple executions are necessary to arrive at a despread result. As stated in Lee:

> A digital processing device processes the received and buffered symbol data by generating a plurality of single process instructions at least at the data rate of the digital data stream, which a sequence of single process instructions is operable to generate despread symbol data.

(Col. 2, ll. 34-44) (emphasis added). Figure 6 shows the instruction of Lee operating on a signal value comprising only a single real bit and single imaginary bit. These bits, referred to as r_I (for the real portion) and r_Q (for the imaginary portion) are part of the same signal value. Therefore the operations performed by Figure 6 show only one signal value being operated on per clock cycle as opposed to the plurality of signal values as required by the claims.

Therefore, Lee does not disclose a single instruction which performs the despread operations of the claims, but rather discloses a system where a plurality of instructions is necessary to despread a signal of multiple real bits and multiple imaginary bits:

> processing the received and buffered symbol data in a digital processing device by generating a plurality of single process instructions at least at the associated data rate, each single process instruction being operable to generate despread data for a given single symbol in the received symbol data;

(Col. 9, ll. 24-30) (emphasis added). See also claims 9 and 16 of Lee.

Furthermore, as shown in figure 6, Lee performs only one complex multiplication. The complex multiplication as shown in Lee is of two two-bit numbers (each with one real bit and one imaginary bit). This operation requires four multiplications and two additions, which is what Lee discloses. This is a single complex multiplication. Accordingly, Lee does not teach, disclose, or suggest a further complex addition of intermediate results to provide a despread result as required by claim 1.

Furthermore, the despread process taught by Lee does not execute within a single clock cycle as required by the claims but rather, since the instruction of Lee can only operate on a single symbol at a time, the system of Lee takes N clock cycles (where N is the spreading factor) to perform the despreading operation:

> With the specialized architecture disclosed herein, the number of clock cycles could be reduced to N...

(Col. 3, ll. 33-35).

Lee, therefore, does not teach, disclose, or suggest a single instruction, which specifies a plurality of signal values, each signal value having multiple real bits and multiple imaginary bits, and a plurality of code segments, and performs complex multiplication, addition and storing all within a single clock cycle as claimed. Lee therefore does not teach, disclose or suggest each element of the claims.

Accordingly, withdrawal of the rejection is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee

occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: July 25, 2007

Respectfully submitted,

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Docket No. A0312.70412US00
Date: July 25, 2007
x6/26/07